I claim:

1. A method for producing a clock output signal, which comprises:

receiving an input signal that contains an information item representing a phase;

producing a plurality of clock signals having phases that are respectively shifted from one another by a predetermined amount;

weighting each one of the plurality of the clock signals in dependence on the information item that is contained in the input signal; and

mixing the weighted clock signals in order to produce a clock output signal having a phase that essentially matches the phase that is represented by the phase information item.

2. The method according to claim 1, which comprises:

producing a clock input signal having a predetermined frequency and a phase;

producing the plurality of the clock signals by shifting the phase of the clock input signal by an amount that is selected

from the group consisting of the predetermined amount and a multiple of the predetermined amount; and

producing the plurality of the clock signals so that each of the plurality of the clock signals has the predetermined frequency.

3. The method according to claim 2, wherein the plurality of the clock signals that are produced are four clock signals whose phases are shifted from one another by 90°.

4. The method according to claim 3, which comprises using a quadrature oscillator to produce the four clock signals from the clock input signal.

5. The method according to claim 1, which comprises performing the step of mixing the weighted clock signals by adding the weighted clock signals.

6. The method according to claim 1, which comprises, when mixing the weighted clock signals, performing band-limiting to filter out harmonics.

7. An apparatus for producing a clock output signal, comprising:

an input for receiving an input signal containing a phase information item representing a phase;

a clock generator for producing a plurality of clock signals having phases that are shifted from one another by a predetermined amount; and

a weighting and mixing circuit for weighting each one of the plurality of the clock signals based on the phase information item to obtain a plurality of weighted clock signals;

said weighting and mixing circuit also for mixing the plurality of the weighted clock signals to produce a clock output signal having a phase that essentially matches the phase represented by the phase information item.

8. The apparatus according to claim 7, in combination with a delay locked loop circuit, said delay locked loop circuit having a delay lock loop control loop including said input, said clock generator, and said weighting and mixing circuit.

9. The apparatus according to claim 8, wherein said clock generator is formed by a quadrature oscillator producing four clock signals having phases that are shifted from one another by 90°; the four clock signals defining the plurality of the clock signals.

10. The apparatus according to claim 7, wherein said clock generator is formed by a quadrature oscillator producing four clock signals having phases that are shifted from one another by 90°; the four clock signals defining the plurality of the clock signals.

11. A control loop, comprising:

a phase shifter for producing a first clock phase;

a phase detector for detecting a phase difference between a second clock phase and the first clock phase, said phase detector producing an output signal based on the detected phase difference;

a charge pump for integrating the output signal of said phase detector, said charge pump having an integration polarity; and

a controller for changing over the integration polarity of said charge pump at predetermined switching points based on the detected phase difference;

the switching points being subject to hysteresis.

12. The control loop according to claim 11, in combination with a delay locked loop circuit, said delay locked loop circuit having a delay locked loop control loop including said phase shifter, said phase detector, said charge pump, and said controller.

13. A method for producing a clock signal, which comprises:

detecting a phase difference between a clock phase of a first input signal for a phase shifter and a clock phase of a first output signal of the phase shifter;

producing a second output signal based on the detected phase difference;

producing a second input signal for the phase shifter by integrating the second output signal; and

changing over a polarity of the integrating at predetermined switching points based on the detected phase difference, the switching points being subject to hysteresis.

14. A charge pump for producing an output signal, which comprises:

a charge pump circuit for receiving an input signal having a phase;

said charge pump circuit also for producing an output signal having a phase;

the output signal selected from the group consisting of a proportional signal essentially proportional to the phase of the input signal and an inversely proportional signal essentially inversely proportional to the phase of the input signal;

said charge pump circuit being designed such that the output signal changes from between the proportional signal and the inversely proportional signal at predetermined switching points at which a predetermined jump in the phase of the output signal takes place.

15. The charge pump according to claim 14, wherein the switching points are subject to hysteresis.

16. The charge pump according to claim 15, wherein the predetermined jump corresponds to a phase return of a predetermined magnitude.

17. The charge pump according to claim 14, wherein the predetermined jump corresponds to a phase return of a predetermined magnitude.